ABSTRACT

A hybrid software/hardware packet filter in which rule
compiling means creates a rule table, assembles packet
acceptance rules, and outputs the acceptance rules to a
configurable hardware circuit to create hardware circuits
representing the acceptance rules and applying the
acceptance rules to the packet and outputting a single bit
for each rule indicating whether the packet matched the
rule. Linking means receives the match bit vector and
links each bit in the match bit vector with the
corresponding entry in the rule table and directs the
packet to a destination determined by the rule table.